FIG. 1

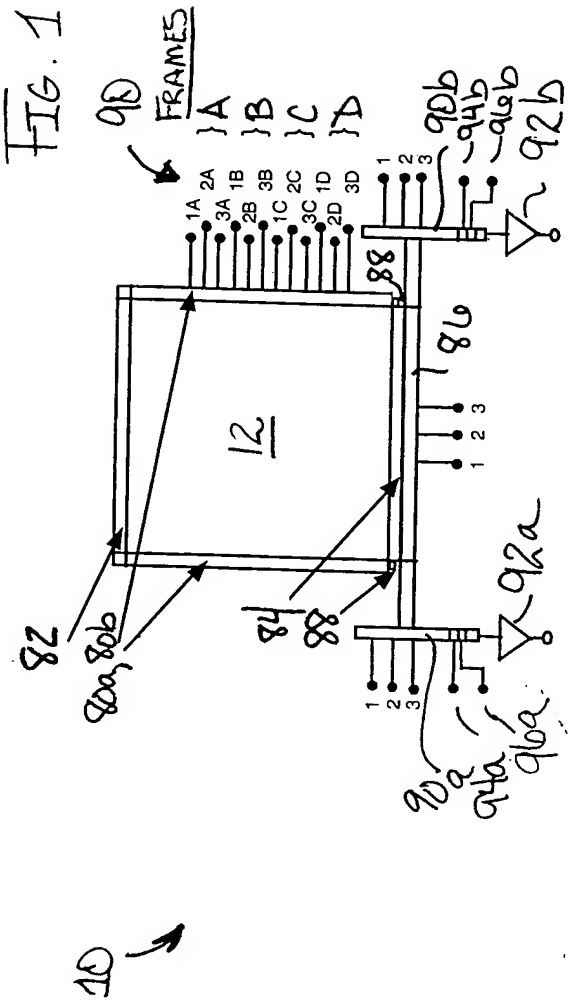
FRAMES
1A
1B
1C
1D
90
1A 2A 1B 3B 2C 1D 3D
1 2 3
90b
94b
96b
92b
88
86
12
1 2 3
92a
82
80a, 80b
84
88
1 2 3
90a
94a
96a
10

FIG. 2A

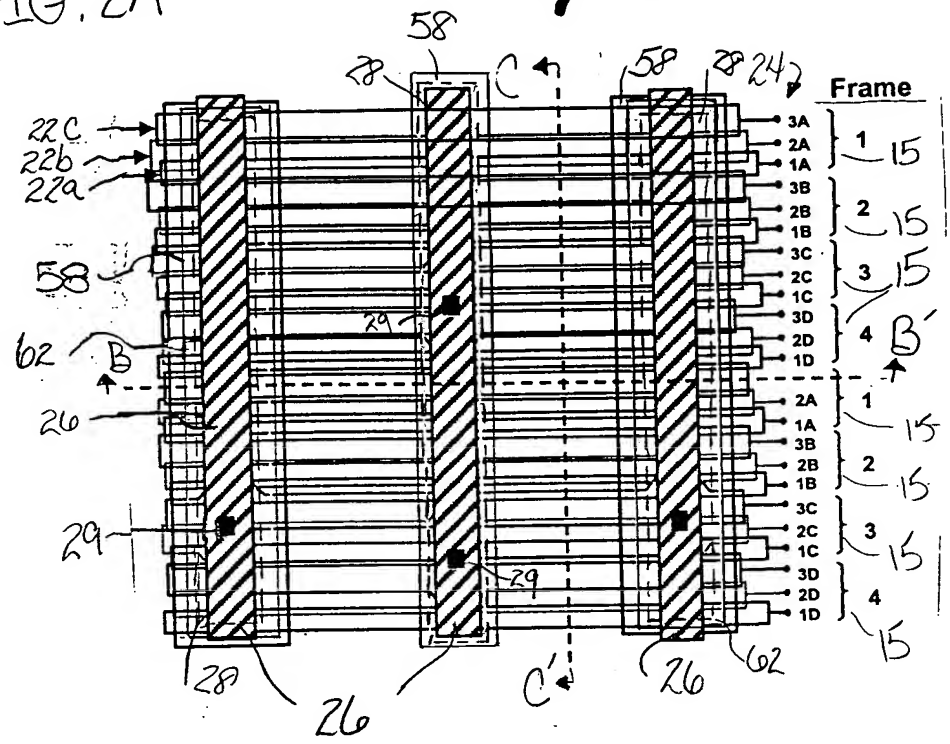

FIG. 2B

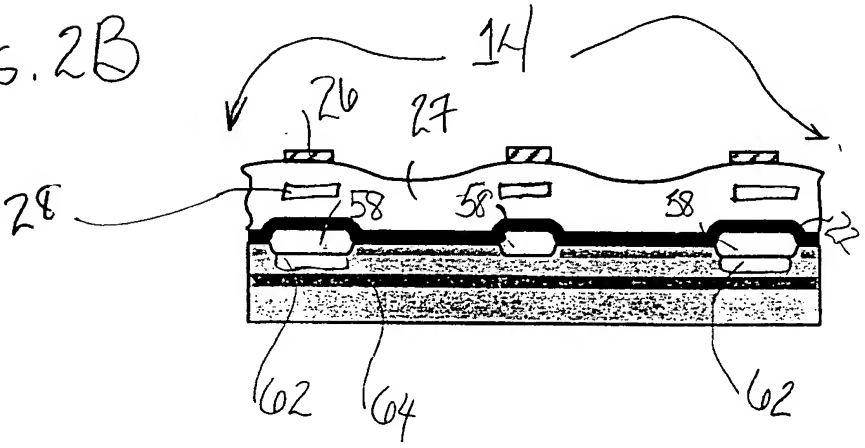

FIG. 2C

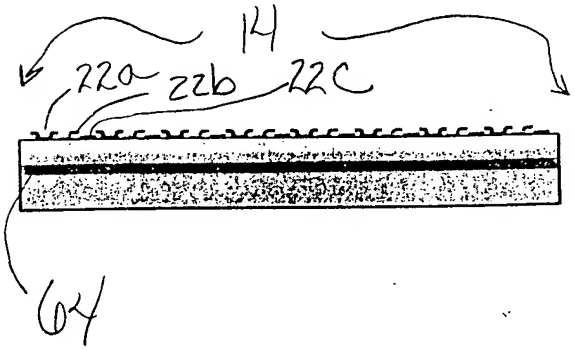

FIG. 3A

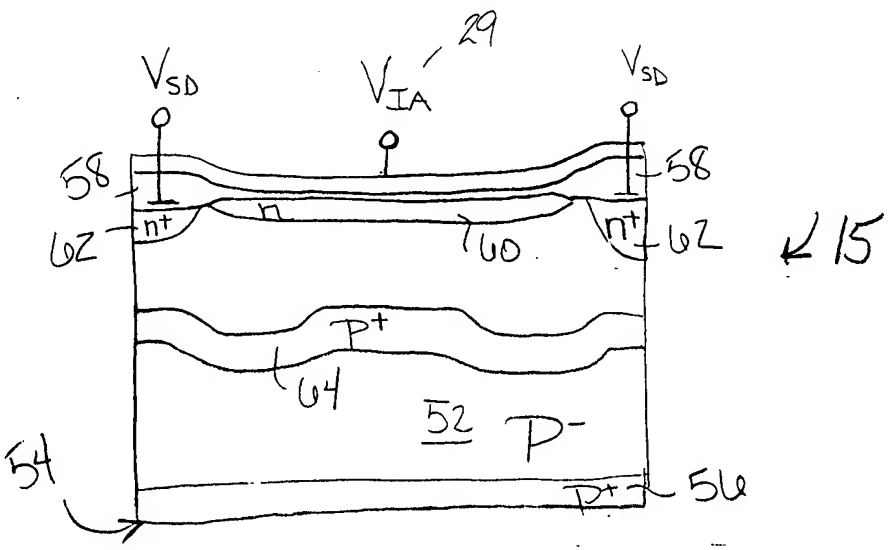

FIG. 3B

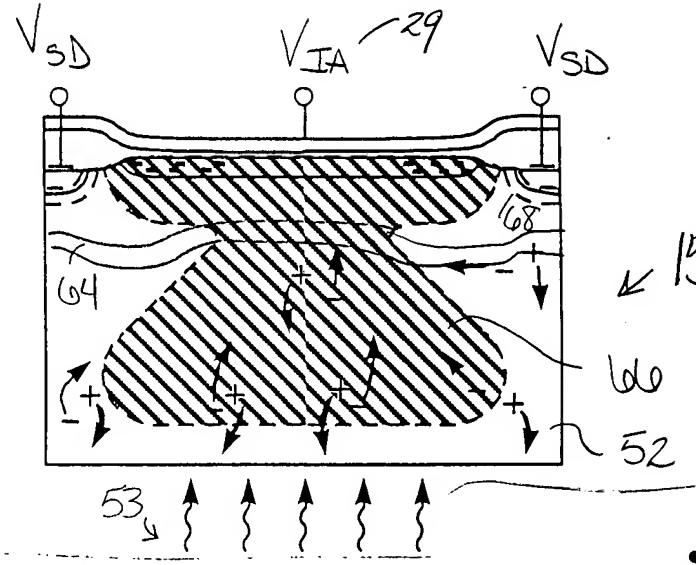

FIG. 3C

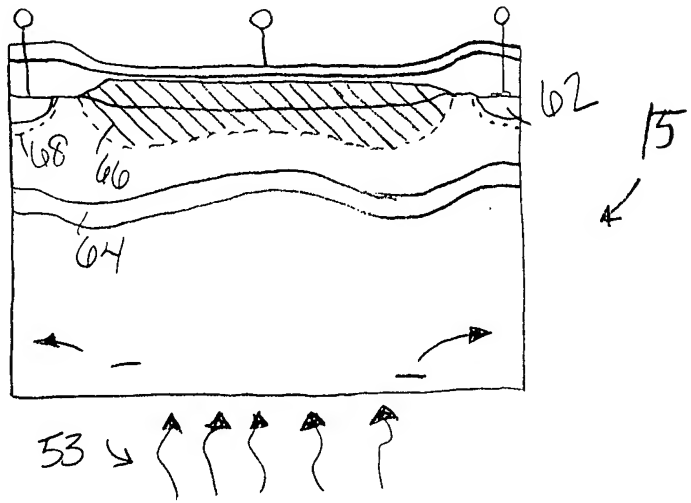

FIG. 3D

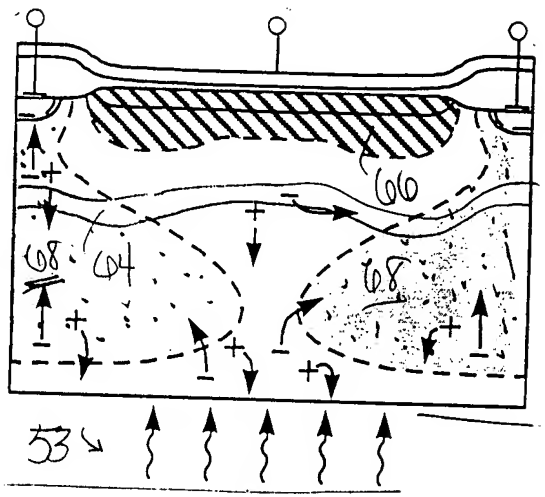

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FIG. 4A

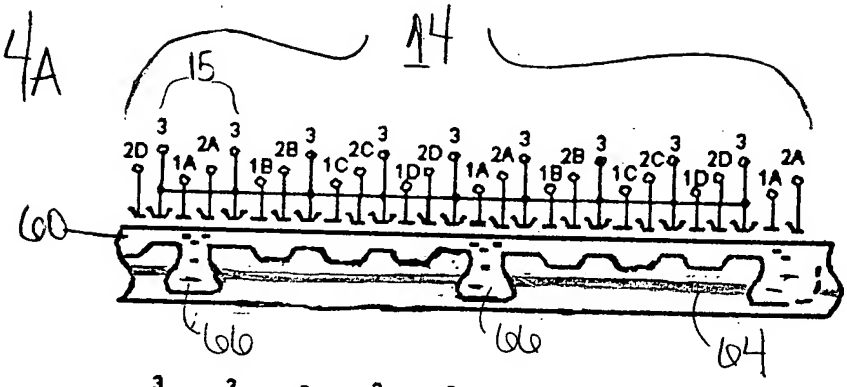


FIG. 4B

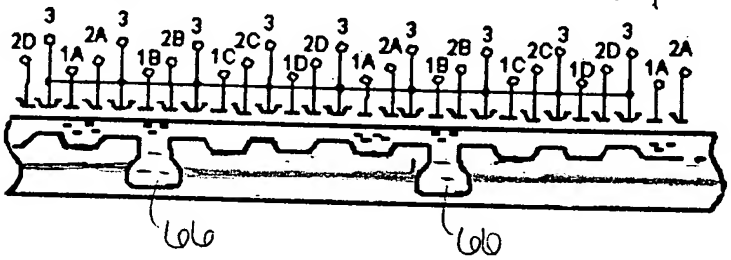


FIG. 4C

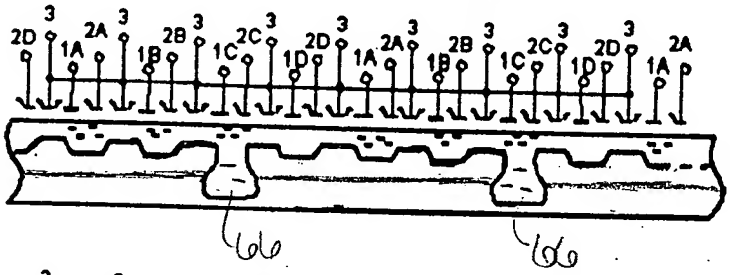


FIG. 4D

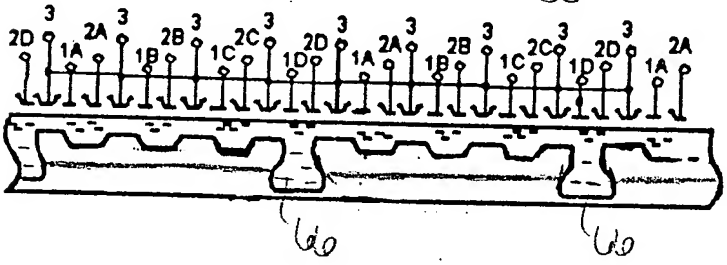


FIG. 5

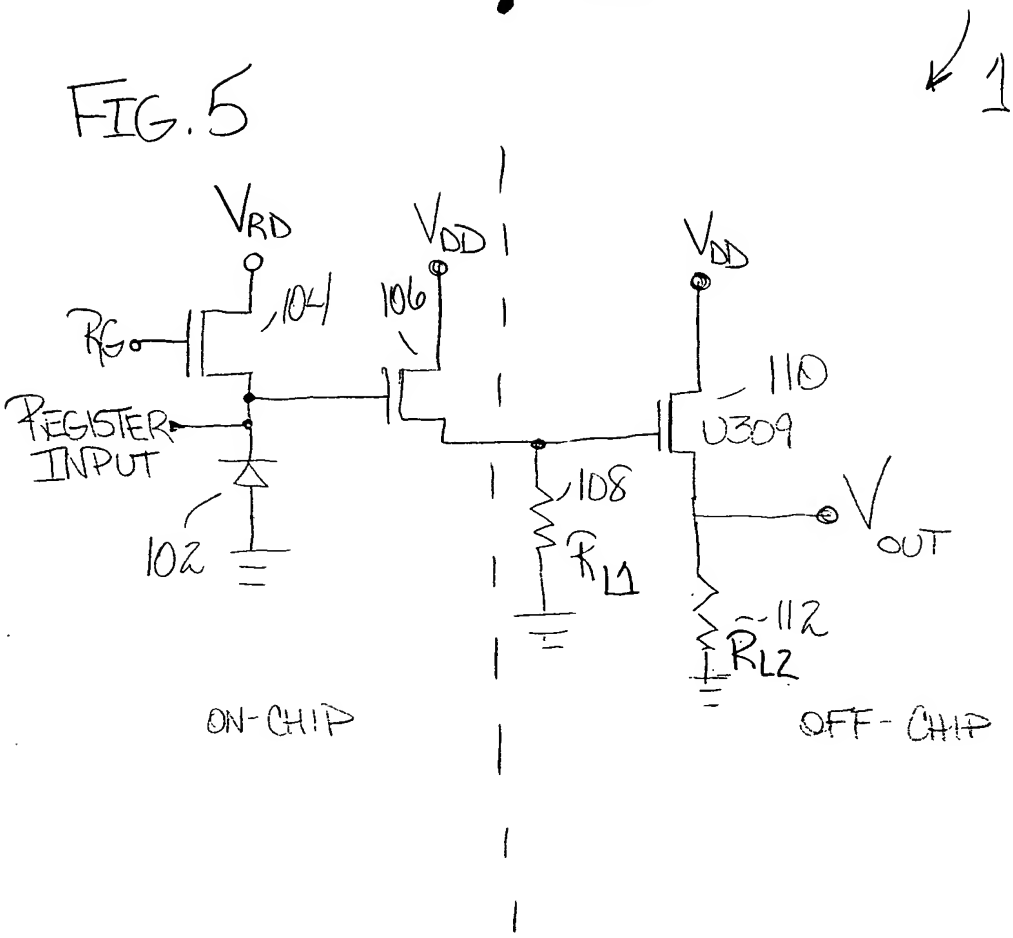


FIG. 8

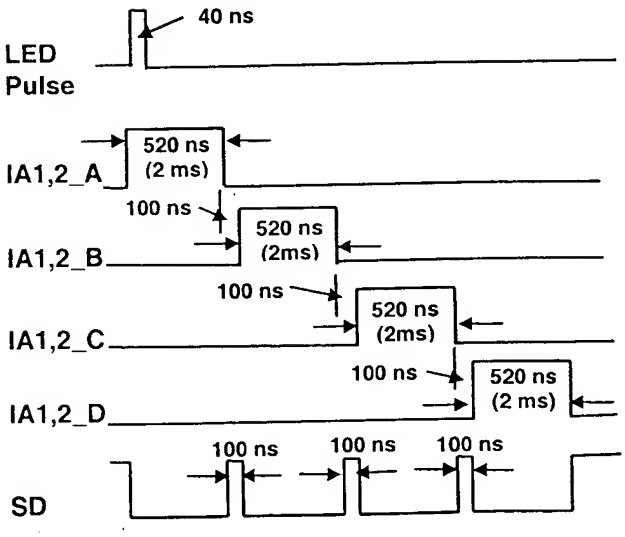


FIG. 9

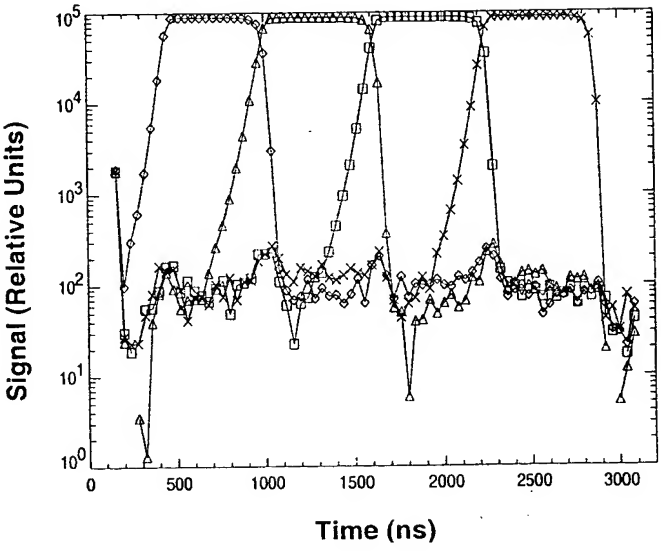


FIG. 6A

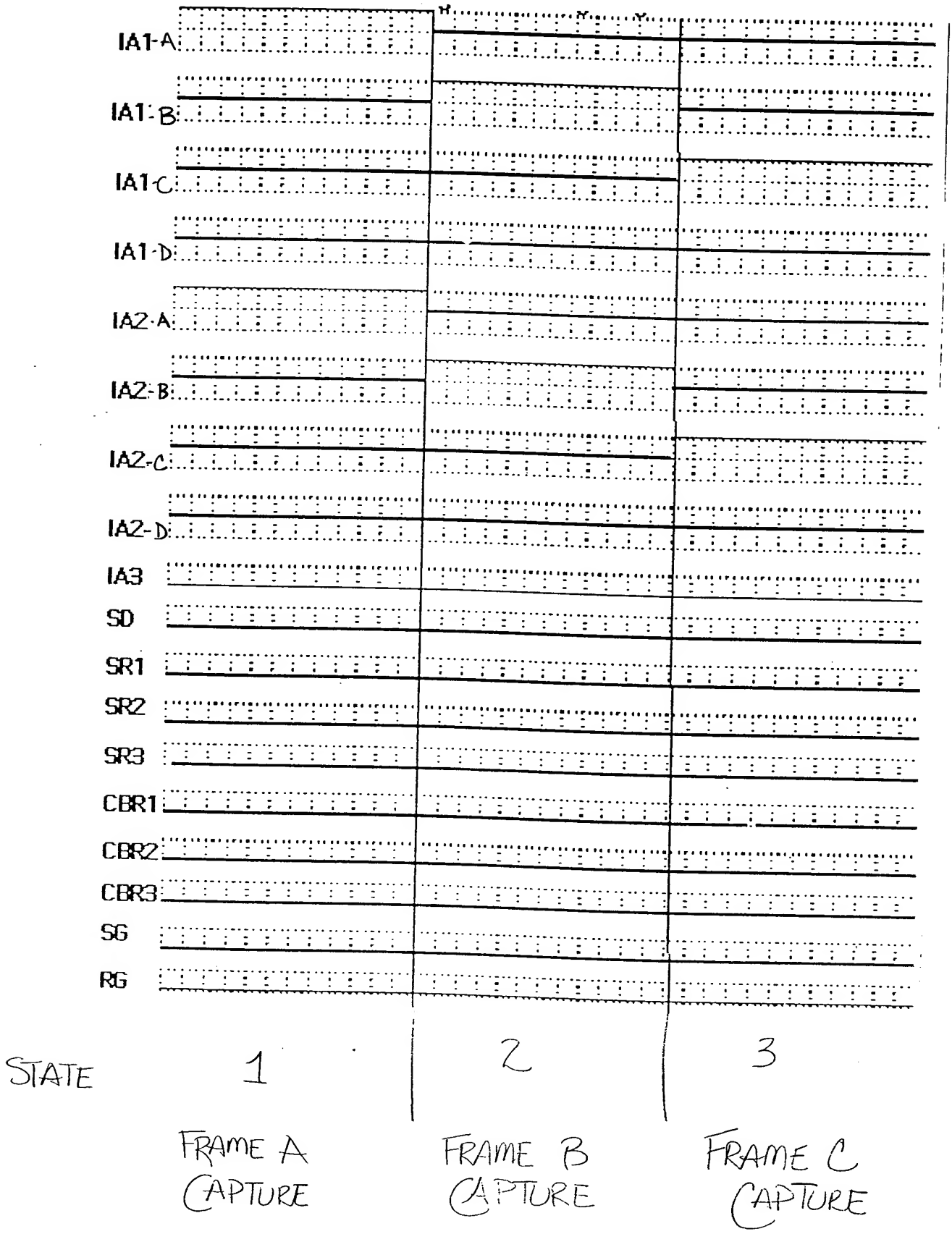

IA1-A
IA1-B
IA1-C
IA1-D
IA2-A
IA2-B
IA2-C
IA2-D
IA3
SD
SR1
SR2
SR3
CBR1
CBR2
CBR3
SG
RG
STATE
1
2
3
FRAME A CAPTURE
FRAME B CAPTURE
FRAME C CAPTURE

FIG 6B

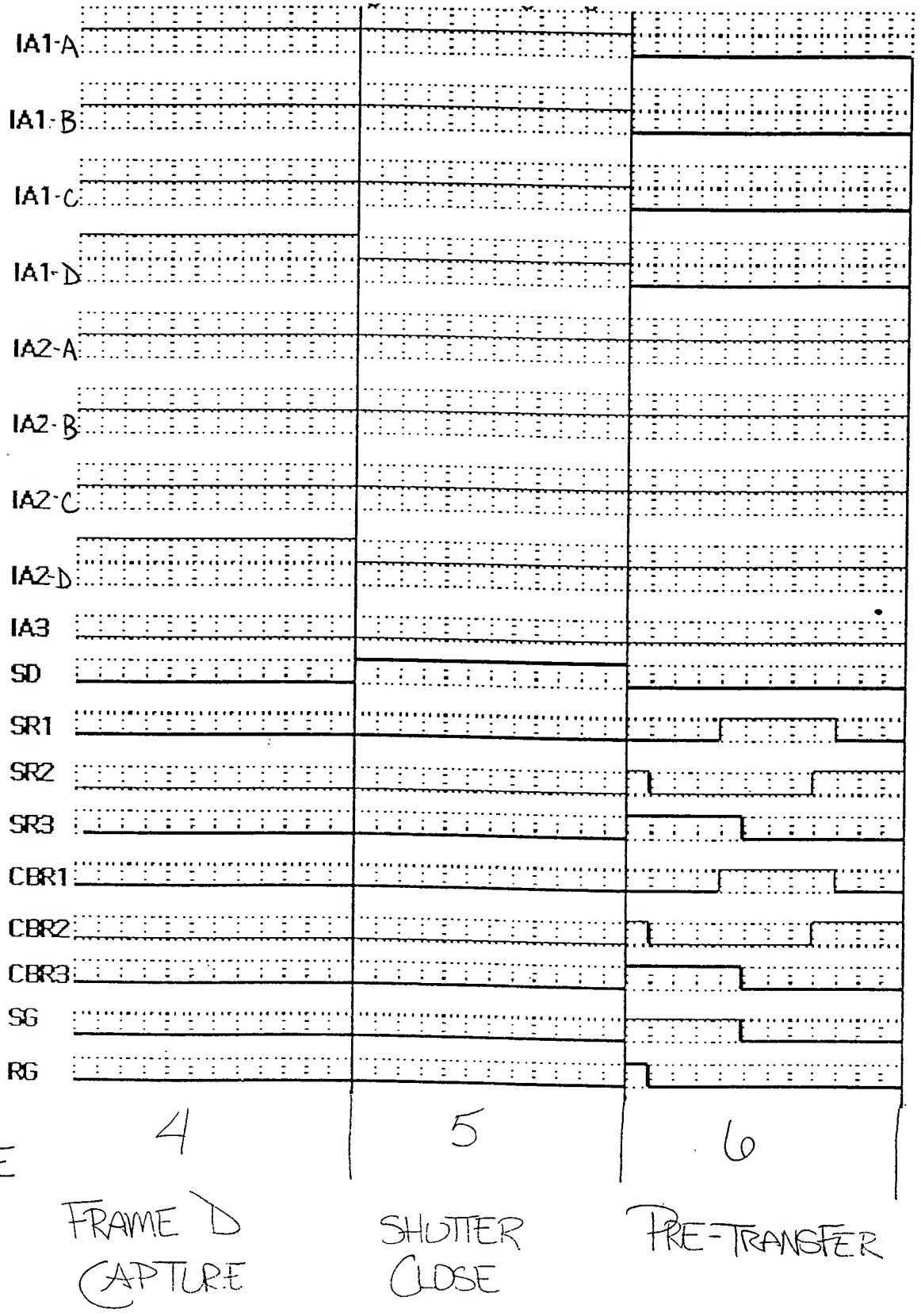

IA1-A
IA1-B
IA1-C
IA1-D
IA2-A
IA2-B
IA2-C
IA2-D
IA3
SD
SR1
SR2
SR3
CBR1
CBR2
CBR3
SG
RG
STATE
4
5
6
FRAME D CAPTURE
SHUTTER CLOSE
PRE-TRANSFER

FIG. 6C

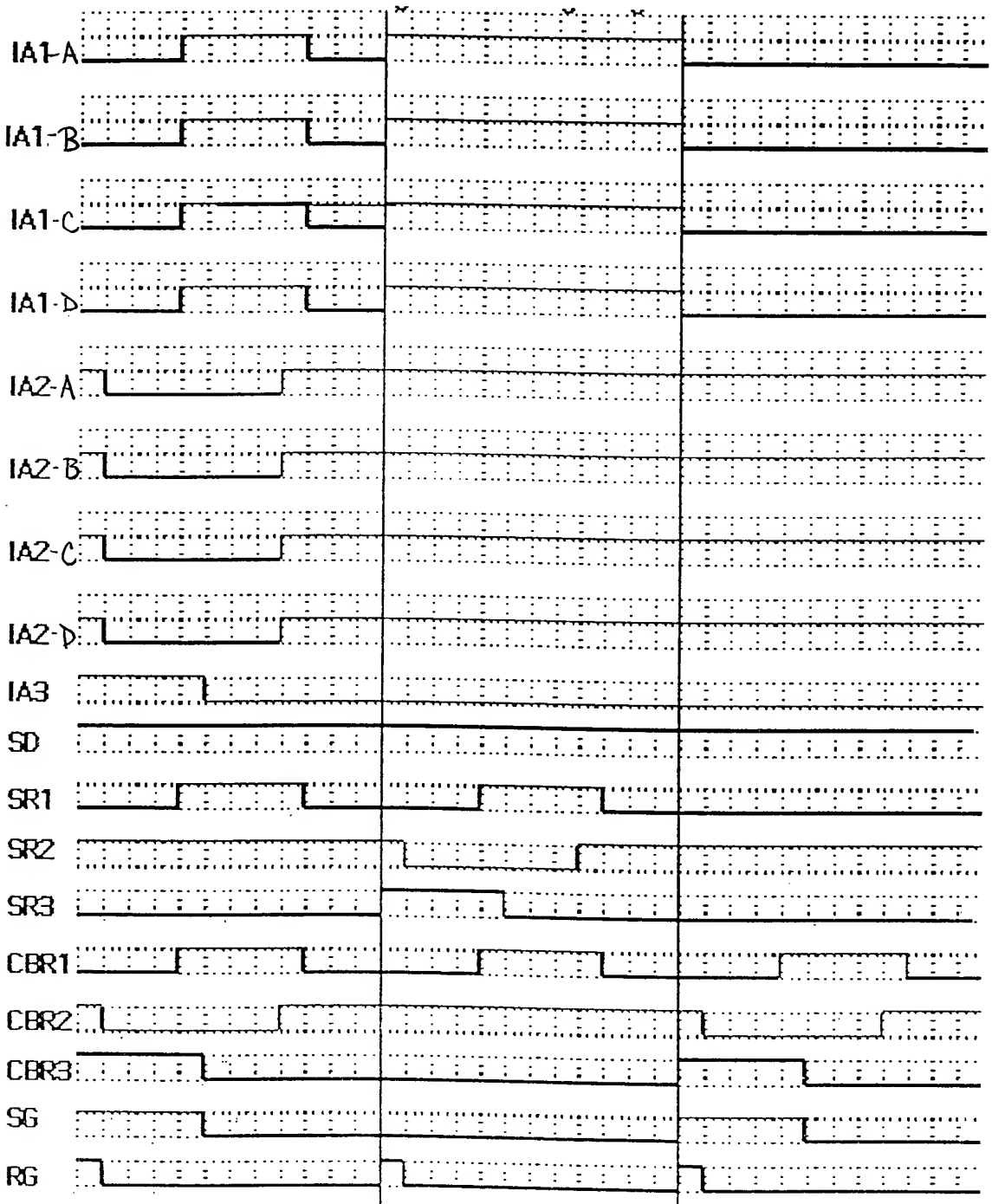
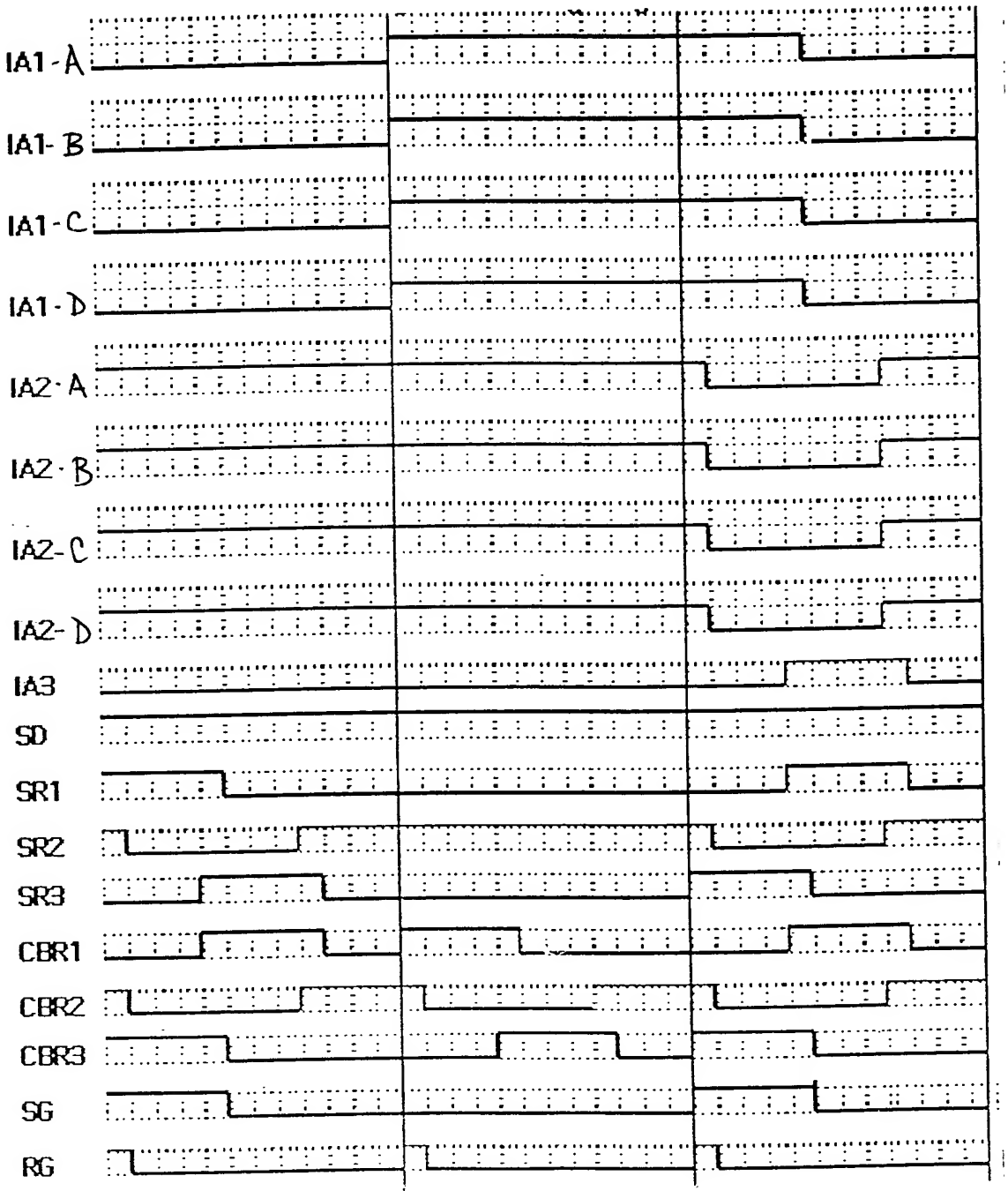

IA1-A
IA1-B
IA1-C
IA1-D
IA2-A
IA2-B
IA2-C
IA2-D
IA3
SD
SR1
SR2
SR3
CBR1
CBR2
CBR3
SG
RG
STATE
7
8
9
SERIAL REGISTER ROW TRANSFER
COLUMN BIN TRANSFER
PIXEL TRANSFERRED OUT

FIG. 6D


IA1-A
IA1-B
IA1-C
IA1-D
IA2-A
IA2-B
IA2-C
IA2-D
IA3
SD
SR1
SR2
SR3
CBR1
CBR2
CBR3
SG
RG
STATE
10
11
12
SERIAL REGISTER ROW REVERSE
COLUMN BIN REVERSE
IMAGE ARRAY REVERSE

150

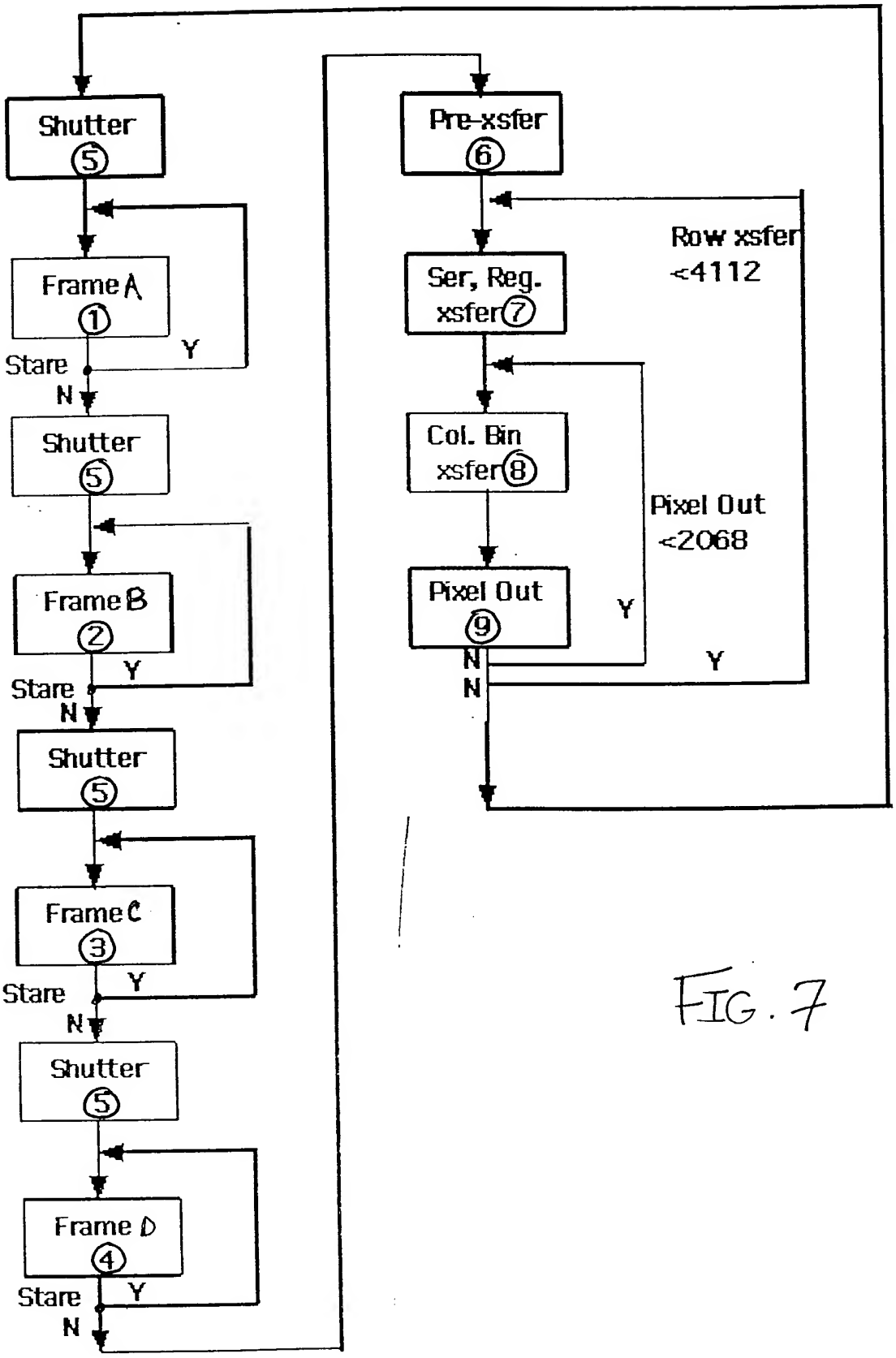

Shutter
5
Frame A
1
Stare
Y
N
Shutter
5
Frame B
2
Y
Stare
N
Shutter
5
Frame C
3
Stare
Y
N
Shutter
5
Frame D
4
Stare
Y
N
Pre-xsfer
6
Ser, Reg.
xsfer 7
Row xsfer
<4112
Col. Bin
xsfer 8
Pixel Out
<2068
Pixel Out
9
Y
N
Y
N

FIG. 7